Amendments to the Specification

Please replace the paragraph beginning on page 1, line 12 with the following amended paragraph:

A FeRAM (ferroelectric random access memory) uses a ferroelectric capacitor. Data can be read quickly from the FeRAM [[FRAM]], which can be operated to provide random access. Therefore the FeRAM is expected as a new type of nonvolatile memory.

Please replace the paragraph beginning on page 1, line 18 with the following amended paragraph:

The FeRAM is classified broadly into [[ether]] either a planar type or a stack type. In the planar type FeRAM, a top electrode of the ferroelectric capacitor is connected to a source electrode of a corresponding switching transistor.

Please replace the paragraph beginning on page 8, line 20 with the following amended paragraph:

First, as shown in Fig. 3(A), the insulating layer 19, the transistor 20, bit line contact [[55]] 32 and the bit line 55 are formed on the semiconductor substrate 12. Then, the insulating layer 13 is formed on the semiconductor substrate 12 and the top surface of the insulating layer 13 is flattened by a CMP(Chemical Mechanical Polishing) technique.

Please replace the paragraph beginning on page 9, line 9 with the following amended paragraph:

Then, as shown in ~~Fig. 3(B)~~ Fig. 3(A), a platinum layer 65 that has 150nm thickness is formed on the barrier metal 17 by a sputtering technique.

Please replace the paragraph beginning on page 9, line 11 with the following amended paragraph:

Then, as shown in Fig. 31(B), a mask M1 such as silicon nitride or titanium nitride is formed on the platinum layer 65. The platinum layer 65 is etched by using the mask M1 so that the projection portion 62b is formed. For example, a size of the projection portion 62b is 1040nm by 800nm and a thickness is 75nm. In this step, a bottom electrode layer 67 which has the projection portion 62b formed on a platinum layer 67a is obtained.

Please replace the paragraph beginning on page 14, line 17 with the following amended paragraph:

Next, a method of fabricating a semiconductor device 200 is explained in reference with ~~Fig. 7~~ Figs. 7(A) – 7(C).

Please replace the paragraph beginning on page 18, line 14 with the following amended paragraph:

The source region 24 is connected to the contact plug 37 and the drain region 26 is connected to the bit line contact 32. The contact plug [[34]] 37 and the bit line contact 32 are formed by embedding a conductive material such as poly crystalline silicon or tungsten in contact holes 33 which are formed in the insulating layer 13.

Please replace the paragraph beginning on page 19, line 18 with the following amended paragraph:

In this embodiment, the capacitor 90 is rectangular in shape. Also, the projection portion [[92a]] 92b is rectangular in shape. Each side of the projection portion 92b of the bottom electrode 92 is shorter than corresponding side of the plate portion 92a of the bottom electrode 92. A side surface "e" of the plate portion 92a, a side surface "f" of the dielectric layer 93, a side surface "g" of the ferroelectric layer 94 and a side surface "h" of the top electrode 96 are aligned with each other.

Please replace the paragraph beginning on page 21, line 15 with the following amended paragraph:

Then, a 100nm thickness platinum layer 106 as the top electrode layer is formed on the strontium bismuth tantalate layer 104 by the sputtering method as further shown in Fig. 13(A). Then, the top electrode layer [[108]] 106, the ferroelectric layer 104, the

dielectric layer 101 and the plate portion 95 of the bottom electrode layer 102 are etched so as to form a ferroelectric structure 110 as shown in Fig. 13(B). The side surface "e" of the plate portion 92a, the side surface "f" of the dielectric layer 93, the side surface "g" of the ferroelectric layer 94 and the side surface "h" of the top electrode 108 are aligned.